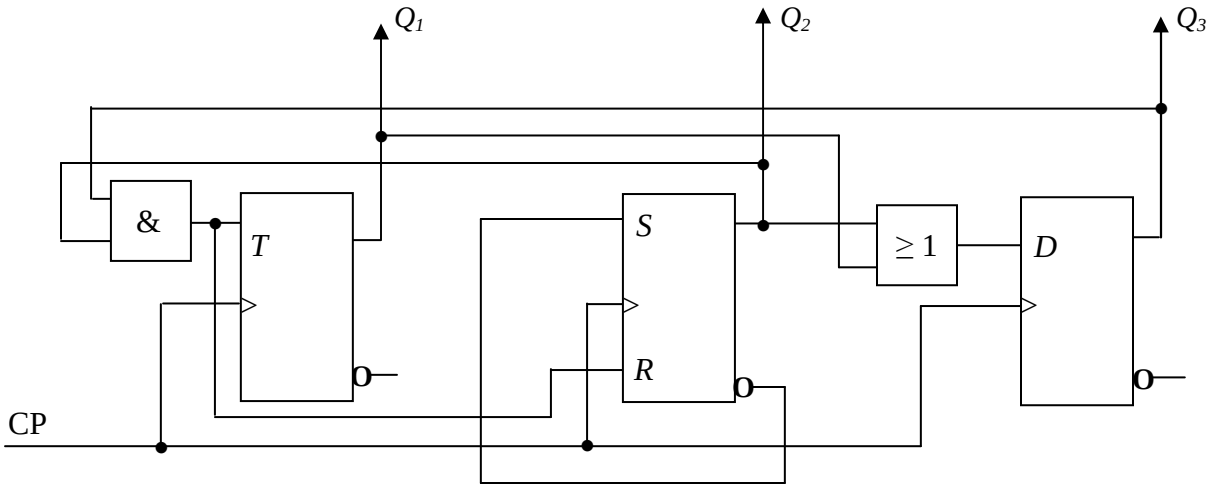
TMEL53 Digitalteknik – Dugga 3 – 15 februari 2012.

TMEL53 Switching Theory and Logical Design – Quiz 3 – 15th February 2012.

1. Beskriv funktionen hos sekvensnätet nedan genom att rita en tillståndsgraf.

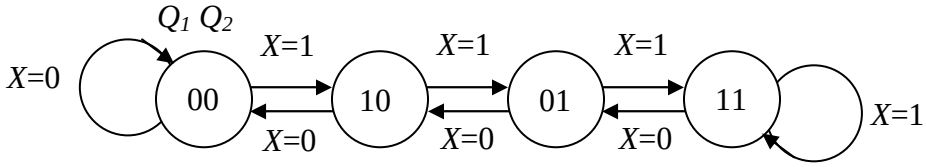
   Describe the function of the sequential circuit below by drawing a state graph.



(5 p)

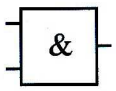
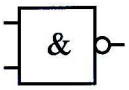
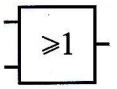
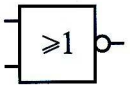
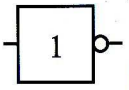
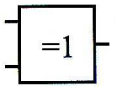
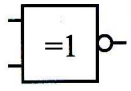
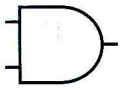
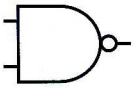
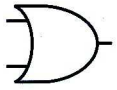
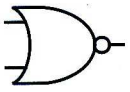
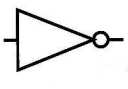
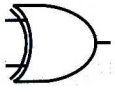
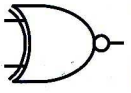
2. Konstruera ett sekvensnät som fungerar enligt tillståndsgrafen nedan. JK-vippor och valfria grindar får användas. För full poäng krävs att konstruktionen är minimal.

   Realize a sequential circuit acting as shown in the state graph below. JK flip-flops and optional gates may be used. To get full points the realization must be as small as possible.



(5 p)

Tabeller över grindar

A	B	$A \cdot B$ AND	$\overline{A \cdot B}$ NAND	$A + B$ OR	$\overline{A + B}$ NOR	$\overline{A}$ INVERS	$A \oplus B$ XOR	$\overline{A \oplus B}$ XNOR
0	0	0	1	0	1		0	1
0	1	0	1	1	0	1	1	0
1	0	0	1	1	0	0	1	0
1	1	1	0	1	0		0	1
IEC								
USA								

Tabeller över vippor

S	R	Q
0	0	Q_0
0	1	0
1	0	1
~~1~~	~~1~~	~~—~~

J	K	Q
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q_0}$

D	Q
0	0
1	1

T	Q
0	Q_0
1	$\overline{Q_0}$

Q	S	R	J	K	D	T	Q^+
0	0	–	0	–	0	0	0
0	1	0	1	–	1	1	1
1	0	1	–	1	0	1	0
1	–	0	–	0	1	0	1